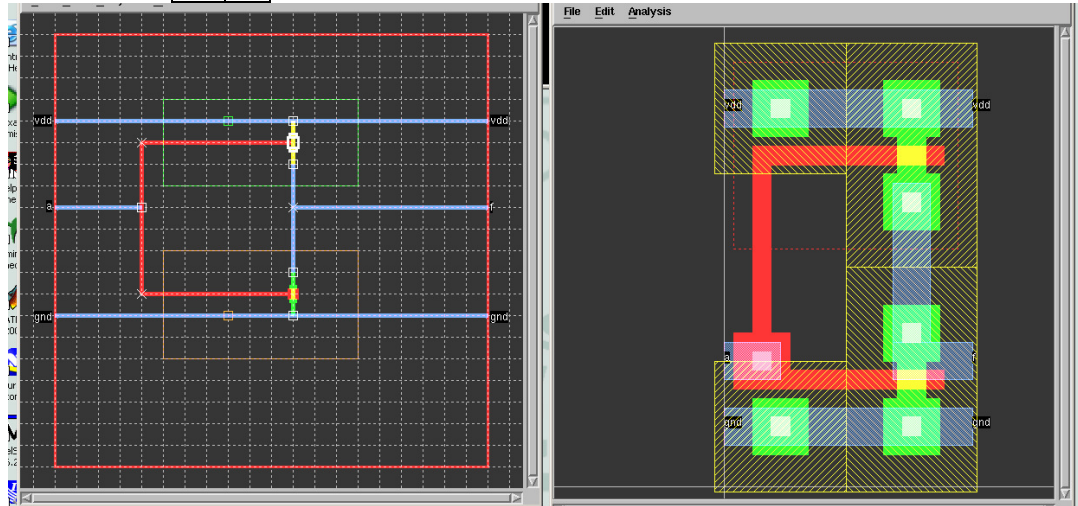


Microelectronics ELEC3260 Computer Aided Design Laboratory report

NOT gate design

The first device created was a CMOS based inverter or NOT gate.

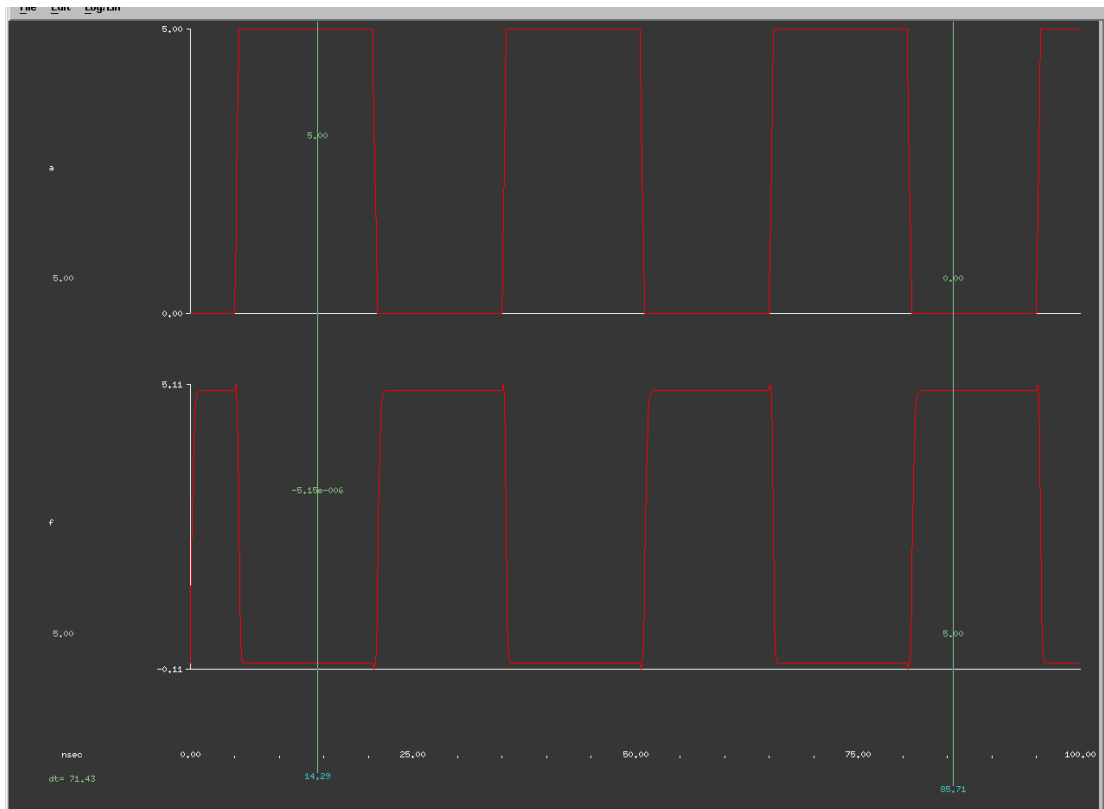
a	f
0	1
1	0



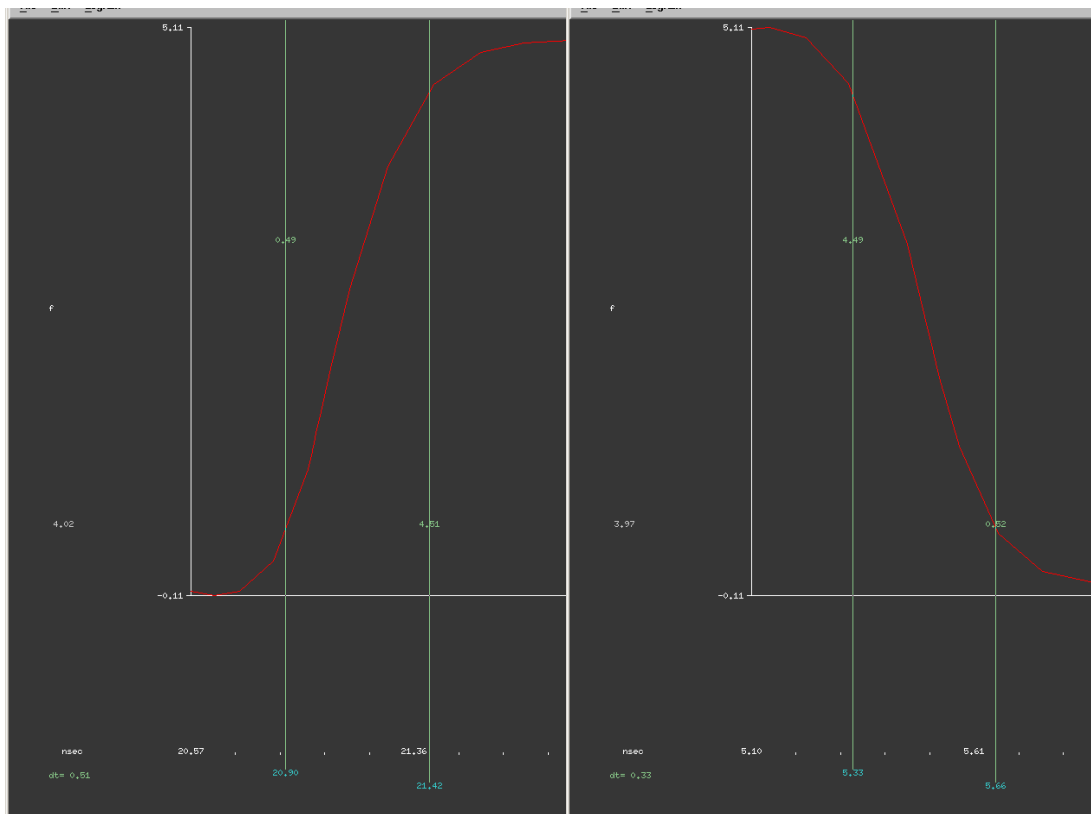
The gate consists of two transistors, the top a P channel device and the bottom an N channel. The output is taken from between the two transistors – effectively like a potential divider. The input is connected as the gate on both transistors. The top metal rail provides voltage supply while the bottom rail acts as the ground.

The device functions as when voltage is high, the top device's gate becomes closed as the positive voltage repels holes and closes off the P channel, while it attracts electrons to the bottom device's N channel. As such, the like that exits at f is electrically connected to ground. When the voltage on input a is low, the P channel of the top device is able to open, while the N channel of the bottom devices closes. The output f is then electrically connected to vdd and is high.

For testing, vdd was set to 5v, gnd to 0v and then input a was pulsed.

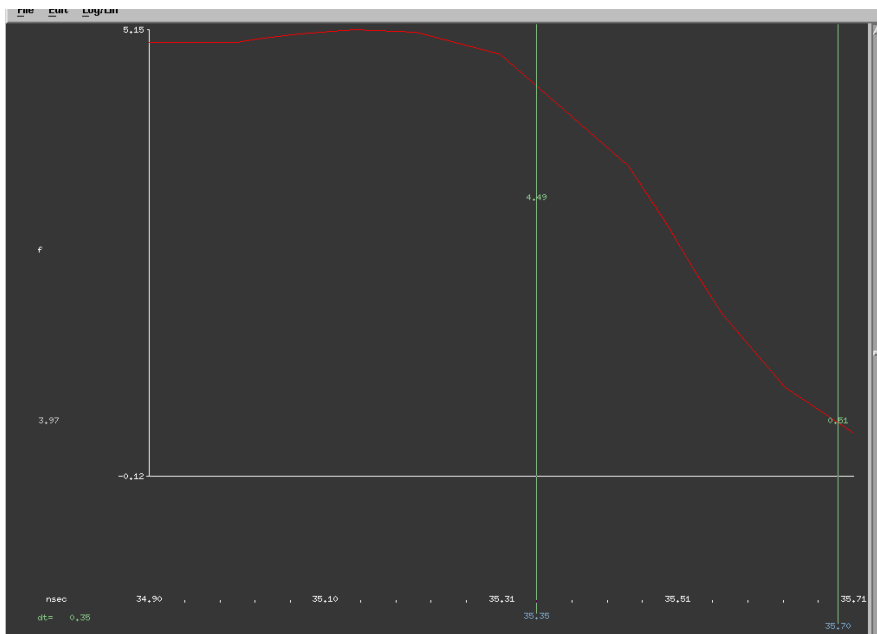
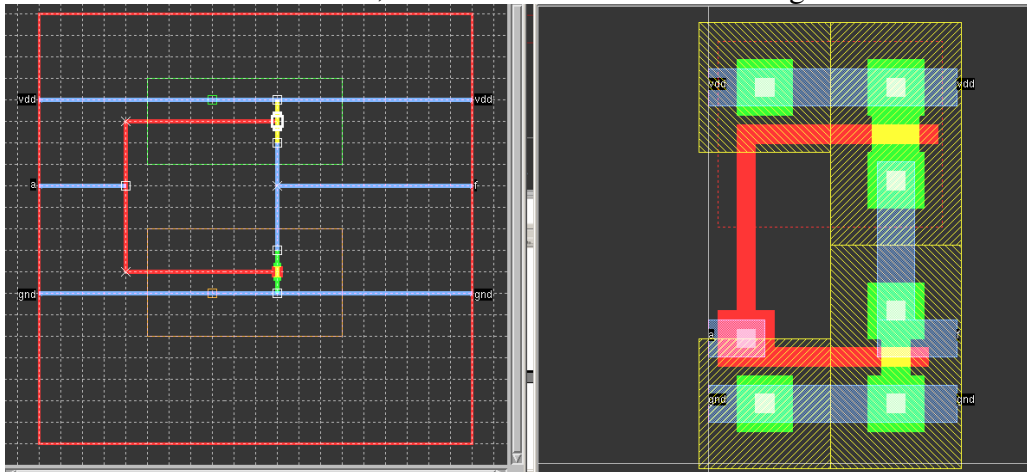


Demonstration of the NOT behaviour of the device

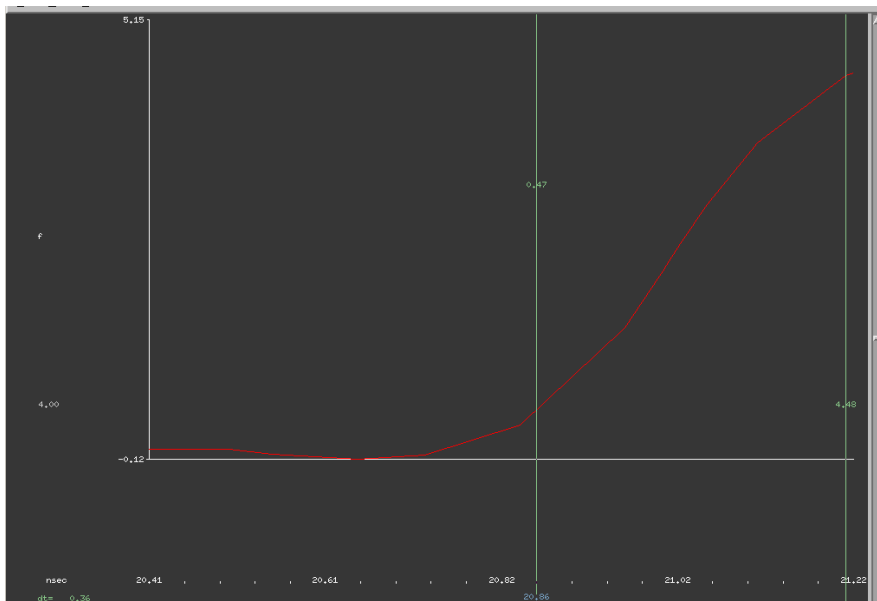


Demonstration of the differing rise and fall times of the NOT gate.

To match the rise and fall times in the inverter's response, the top P channel device (which acted slower due to hole mobility being less than electron) was widened from 3 to 5 microns, with the N channel device being left at 3 micron width.



Fall time

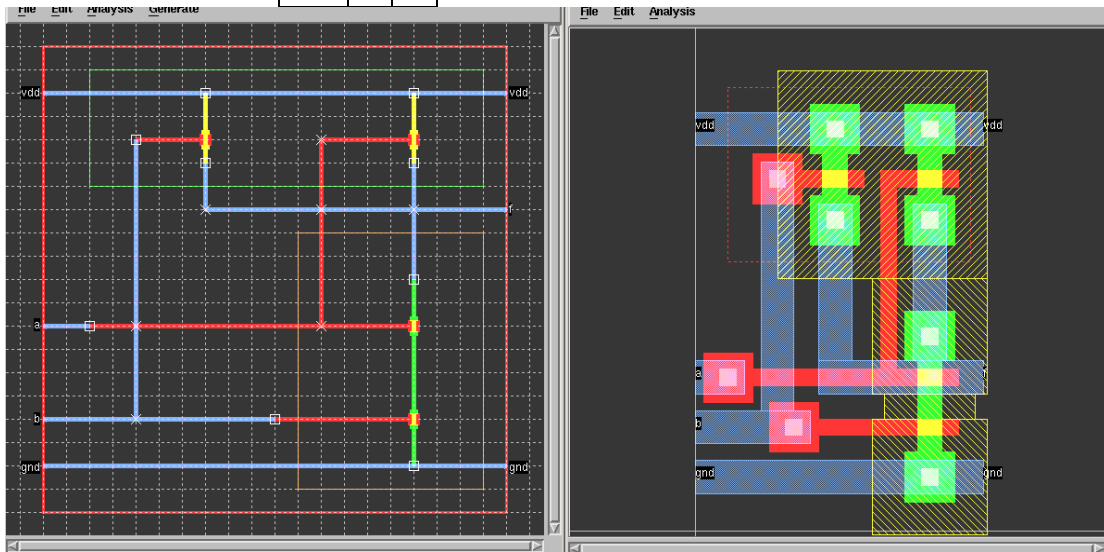


And equal rise time

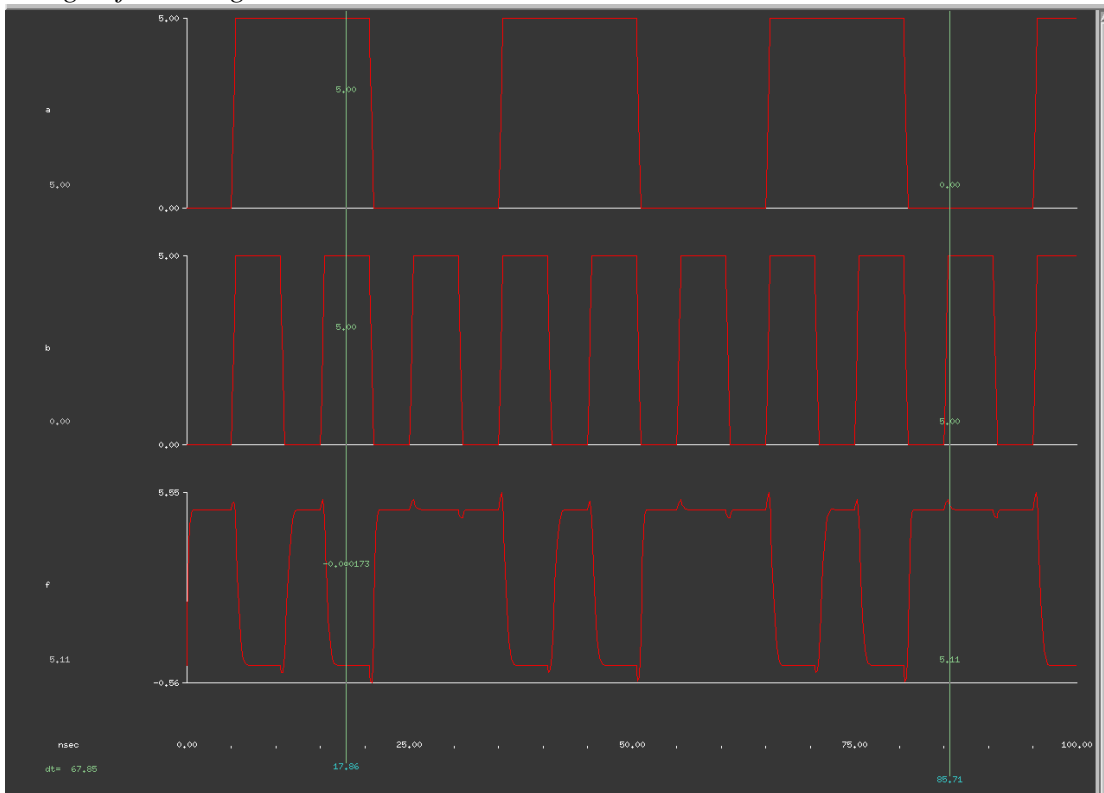
NAND Gate design

Second device was a dual-CMOS NAND gate.

a\b	1	0
1	0	1
0	1	1



Design of NAND gate.



Demonstration of NAND behaviour – output is high in all situations except both inputs high.