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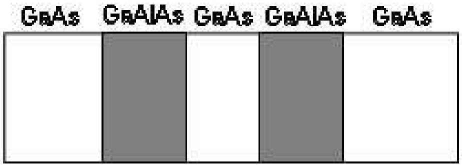
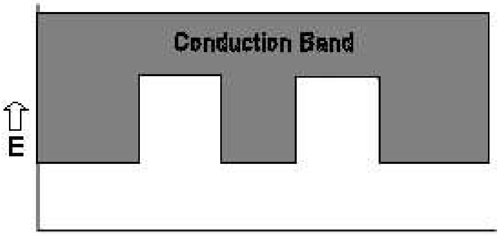
Report on the Fabrication of Resonant Tunnelling Devices.

Overview

The aim of the project was to fabricate a collection of resonant tunnelling devices on a gallium arsenide substrate in the clean room. This required the learning and use of a collection of fabrication techniques in order to produces the desired end product. It also served as a learning process in the possibility of fabricating future devices.

Device theory and concept





The resonant tunnelling device only allows current flow at specific voltages – this produces a very unusual and distinctive voltage-current behaviour that is in no way ohmic. By inserting 1.7nm layers of Gallium Aluminium Arsenide into the device, the energy levels of the conduction are changed. In fact, the GaAlAs conduction band is so much higher than that of GaAs that the electons cannot pass unless a very large voltage is applied. However, the phenomena of quantum tunnelling means that there is a chance that some electrons will pass. Alone, the thin GaAlAs barrier would do little, but by sandwiching a 4.5nm layer of GaAs in between, there are certain unique effects. The size of the layer and the wavelike properties of electrons mean that electrons can only exist at certain energy levels within the layer. These energy levels are the De Brogli wavelength of electrons that can form a standing wave within the layer. The likelihood of electrons tunnelling the 1.7nm into the GaAs sandwich layer is much greater than that of electrons tunnelling the 7.9nm across the whole sandwich. Hence, current and electrons only passes when the energy of the electrons (the voltage applied) is equivalent to the standing wave values. The Diagram shows the layered structure of the RTD along with an energy band diagram for that specific location.

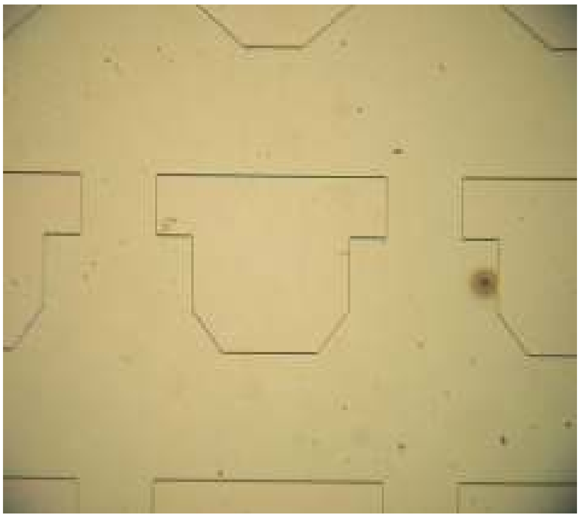
For the purposes of this practical the layers were formed into the wafers used by molecular beam epitaxy before we began any further processing upon them.

Processing Techniques

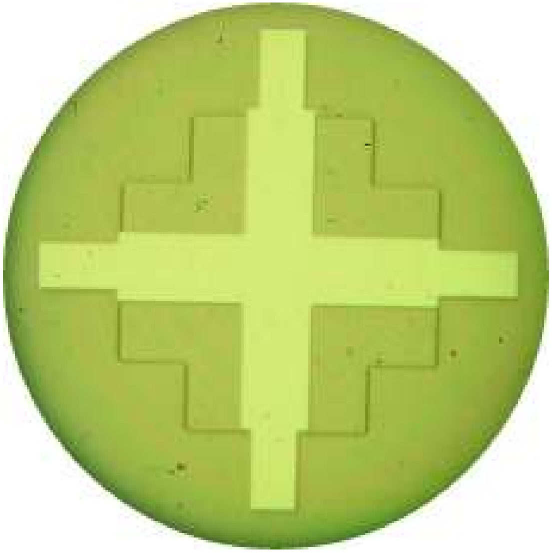
Having obtained the small (approx 1cm by 1cm) square cut wafers with the layers of doped GaAs, GaAlAs and GaAs on, the first stage was to “spin on” the photoresist to be used to pattern the device. The resist used throughout this fabrication was Shipley 1813. This was achieved by placing a small quantity of liquid resist on the wafer and then rotating it at 3000rpm for 30 seconds. This left a very thin layer of resist on the wafer. The thickness of this resist could doubtless be altered by the spin speed, the viscosity of the resist and the strength of interactions between the substrate and the resist solution. The sample was then baked at 110°c for 60 seconds. This hardened the resist from liquid to soft solid.

The next stage was to perform the first alignment and exposure. The wafer was placed into the alignment device, that held the wafer and allowed for rotation, and allowed the user to view the current status of the wafer under an optical microscope. For this stage, it was sufficient to merely align the edge of the wafer with the edge of the mask – still quite accurately however. Then the resist was exposed to UV light through the mask. In this case the area of resist exposed to the UV light was weakened and could be broken down by the developer. The wafer was then placed in developer solution for 60 seconds and the exposed resist removed, then the wafer was washed and dried for the next stage.

Etching the wafer was then required, to produce the area of raised 'mesas' that would form the bulk (although not perform the function) of the main device. To perform the etch, the wafer was immersed in a mixture of Sulphuric acid, hydrogen peroxide and water. Then, after approximately 2 minutes 10 seconds the wafers we removed and washed off. Finally, the remaining resist was removed using acetone – this breaks down even the exposed/unexposed resist, leaving the wafer exposed again. The image here shows an optical microscope image of one of the decahedral mesas after etching.



Next phase involved once again spinning on a layer of resist and baking it in an identical way to before. This time around however, the alignment had to be very precise, as the majority of the wafer would be etched away, leaving a few precisely position raised strip-like mesas on each of the decahedral mesas. The precise alignment was achieved by careful adjustment in both x and y directions and θ rotation to position careful over a pre-designed alignment mark (or rather several of them across the wafer) rather than against any of the functional structures. Once again, after exposure to UV light a developer solution removed the excess resist, just protecting the desired small areas from etching. The image here shows an alignment mark correctly aligned with the mask (silver).



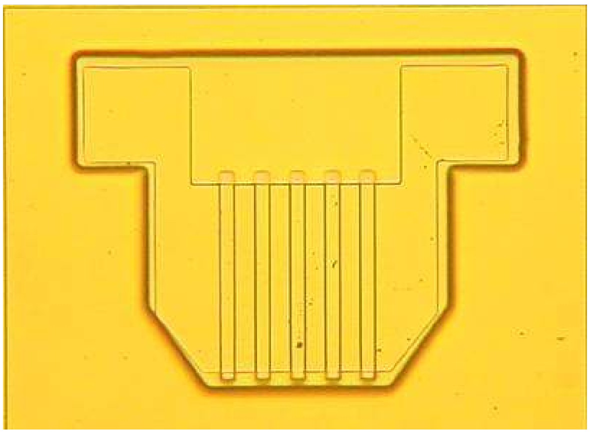
Another etch was performed using

the $H_2SO_4/H_2O_2/H_2O$ mix, this time for a shorter period. No images available here, but it looks similar to the image after the first etch save with between one and five vertical lines of varying length at the bottom of the larger mesa.

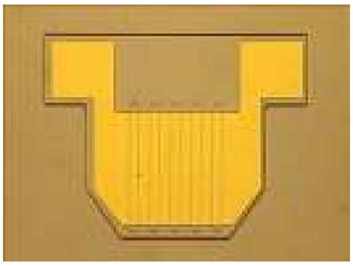
Another stage, another layer of 1813 resist spun and baked on to the wafer.

Exposure three requires an even more precise alignment so as to ensure the metal is laid down in the correct position. This was again based around ensuring all the alignment marks across the wafer were in exactly the correct position with respect to the previous layers.

In this case however, rather than proceeding directly to development, the resist-coated wafer was first soaked in chlorobenzene. This has the effect of hardening the top micron or so of the resist (as far as the chlorobenzene can penetrate). As a result, after the wafer was placed in neat developer (rather than the solution previously used) the developer slowly ate away at the top micron or so – but after reaching through this depth, could expand and erode rapidly. This has the effect of creating and under hang in the resist. When the metal was laid down in the future process, there would be no connection between the metal on the resist and the metal on the wafer. Removing the resist should not then tear the metal from the substrate too.



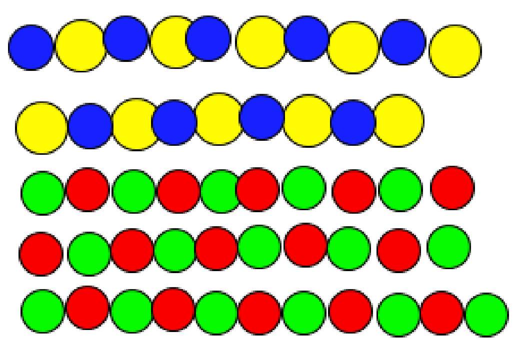
Metal was then applied to the wafer through the process of evaporation. For this, the wafer is placed in a vacuum chamber with the face requiring coating pointed towards the sources. The sources consist of a filament (typically tungsten) coated in the metal desired to coat. The filament is then heated to boil the metal coating which will deposit on the chosen substrate. The change in frequency of vibrations of a quartz crystal (also exposed to the evaporated metal) allows monitoring of the thickness of metal deposited. In the case of our RTD covered wafer, there were a series of evaporations. Initially a very thin (2-8nm) layer of nickel to 'wet' the sample, then a considerable layer of gold-geranium (50-70nm), a blocking layer of titanium (100nm) (purpose to be explained in alloying section) and then a final surface layer of gold (~200nm). The image here shows the device after evaporation.

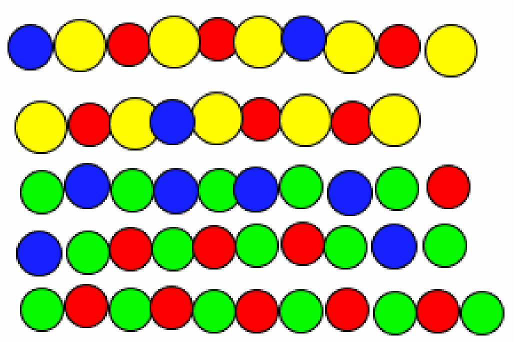


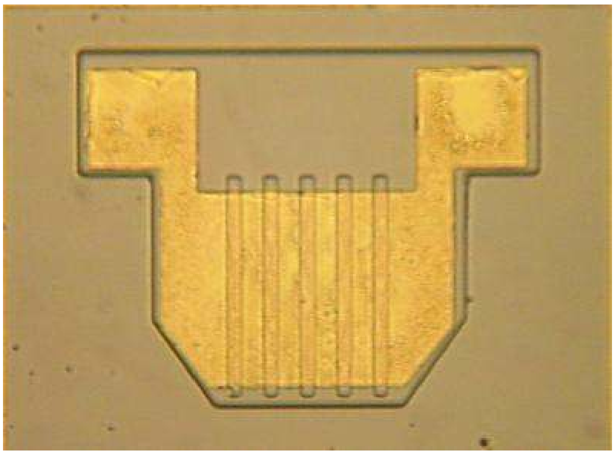
A treatment in acetone to remove removes the resist, and the gold attached to said resist, leaving the structure much like this. Note – while it may appear a solid band of gold, there is **no** continuous connection between the gold on higher mesas (thin vertical strips) and on the lower mesa. This is critical for functioning of the device – if the gold was continuous, the electrons would simply conduct through the gold, bypassing the RTD.

However, there is a problem in the contact between the gold and doped gallium arsenide. Much like the doped GaAs and the GaAlAs have different band gaps and different energy levels for the bottom of the conduction band, so do gold and doped GaAs. To get electrons to climb this barrier therefore requires a way of adding a gradient rather than an abrupt step. The process of alloying then becomes significant. The wafer was placed in a nitrogen-rich oxygen-free environment, and then heated to

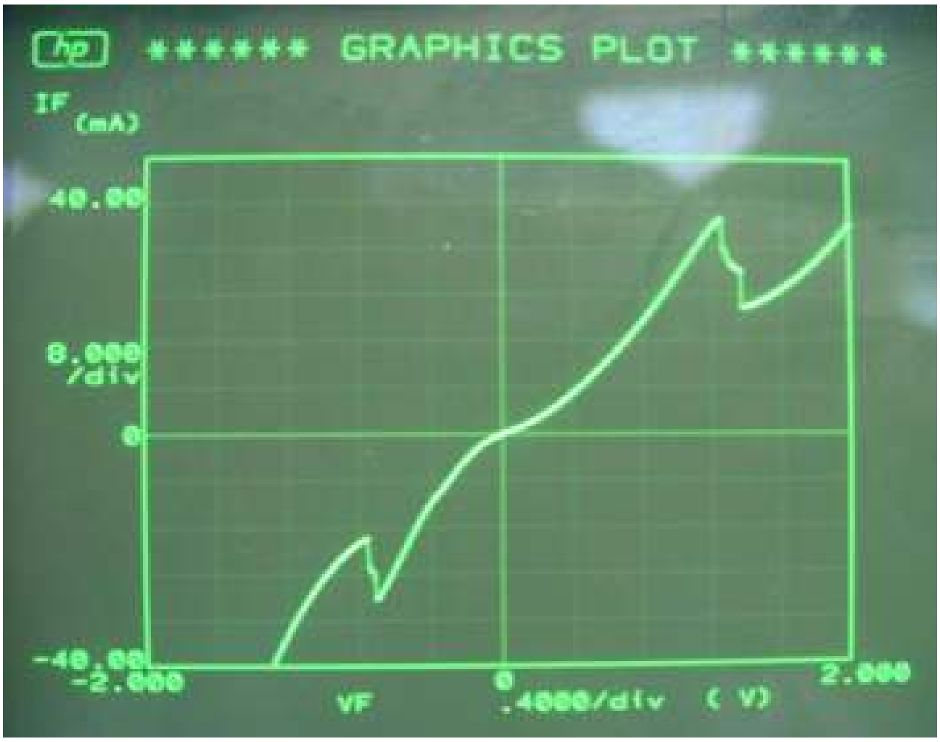
400°c. The lack of oxygen prevented any oxidation reactions. In this time, the geranium from the evaporated gold geranium material defuses into the semiconductor and occupies sites in the crystal structure. This adjusts the band gap of the semiconductor again providing a gradient for electrons to cross rather than a barrier. At the same time, replaced atoms from the semiconductor defused into the gold lattice, as shown in the 'before' and 'after' diagrams here. The semiconductor atoms were prevented from reaching the exposed surface however by the titanium layer. The top surface therefore stayed pure gold, and will not oxidise and compromise its conductive performance. The image here shows the RTD after the annealing process.







After all these steps, it is possible to actually test the device and look for the trademark resonant tunnelling behaviour. By connecting one probe with the raised mesas and another two the gold pads on the lower mesa, a bias can be applied and the behaviour of the device observed.



The graph here shows the voltage against current through the device. As can be seen, the current slowly rises with the voltage, then increasing more rapidly as approaching the resonant energy level. Having past the resonant energy, current decreases rapidly again. More resonance levels theoretically exist, but it is very likely that the device would melt before voltages were high enough to achieve this.

At this stage the devices are functional, but incomplete. To enable easier use of the device, a resist ‘bridge’ would be formed from below the device (as seen on the page) to the raised small mesas. A gold ‘finger’ contact would then be laid over this bridge – and this particular section of resist should not be removed. This finger would link down the contact pads below. Masking, developing etcetera techniques would be largely repeats of those above.

Almost certainly the greatest cause of failure among the devices was caused by misaligned, often only slightly exposures. Naturally, alignment would improve with practice, but this is still a problem. Perhaps some kind of automated alignment and exposure system would be of use. In addition, many of the wafers lost all their gold after immersion in acetone. This suggests that timing with regards to the chlorobenzene and developer on the exposure/development stage of the metal lay-down perhaps needs some refinement.